IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Atty. Docket

ARTHUR TRITTHART ET AL DE 000181

Serial No.

Filed: CONCURRENTLY

METHOD FOR THE SELECTION (PUNCTURING) OF DATA BITS

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

IN THE CLAIMS

Please amend the claims as follows:

3. (Amended) A method as claimed in claim 1, wherein the data bits selected within one cycle of operation are counted.

5. (Amended) A method as claimed in claim 2, wherein the data bits that are already present in the buffer memory which is constructed as a shift register are shifted through the number of new data bits prior to the writing of new data bits.

6. (Amended) A method as claimed in claim 1, wherein the selected data bits, possibly already present in the buffer memory, are prepared so as to form an output data word, while utilizing a working bit register which contains m working

bits and defines the output format, for output to a memory or the like.

8. (Amended) A method as claimed in claim 6, wherein a predetermined number of data bits is output from the buffer memory.

9. (Amended) A method as claimed in claim 6, wherein the data word read out from the buffer memory is extended by the addition of one or more further data bits.

10. (Amended) A method as claimed in claim 6, wherein the data word read out from the buffer memory is shifted within the output data word.

11. (Amended) A device for carrying out the method claimed in claim 1, including a working processor (2) and a data bit selection unit (1) for selecting one or more given data bits from a data word (4), comprising n data bits (10), on the basis of a selection bit register (6) which contains n selection bits (11) which indicate whether a data bit (10) of the data word (6) is to be selected, such selection taking place within one cycle of operation of the working processor (2).

13. (Amended) A device as claimed in claim 11, characterized in that there is provided a buffer memory (7) which is constructed as a shift register and in which the data bits (10) selected within one cycle of operation can be stored.

14. (Amended) A device as claimed in claim 11, characterized in that there is provided a counter for counting the data bits (10) selected within one cycle of operation and for summing the numbers of bits of a plurality of cycle of operation.

15. (Amended) A device as claimed in claim 13, characterized in that data bits already present in the buffer memory (7) can be shifted in dependence on the number of new data bits (10) to be written.

16. (Amended) A device as claimed in claim 11, characterized in that there is provided at least one working bit register (8) which contains m working bits (14) and defines the output format, said working bit register preparing data bits read out from the buffer memory (7) so as to be output in the form of an output data word (9).

18. (Amended) A device as claimed in claim 16, characterized in that there is provided a second counter section (II) which defines the number of data bits (13) to be read out from the buffer memory (7).

19. (Amended) A device as claimed in claim 16, characterized in that there is provided a third register section (III) whereby the data bits (15) read out can be shifted within the output data word (9).

20. (Amended) A device as claimed in claim 16, characterized in that there are provided a fourth and a fifth register section (IV, V) which define how the output data word (9), consisting of m data bits (15), is to be completed when n data bits are read out from the buffer memory (7), where $n < m$.

21. (Amended) A device as claimed in claim 16, characterized in that there is provided a sixth register section (VI) whereby the output mode can be adjusted.

23. (Amended) A device as claimed in claim 11, characterized in that it forms part of a portable telecommunication device for mobile telecommunication.

REMARKS

The foregoing amendments to claims 3, 5-6, 8-11, 13-16, 18-21 and 23, were made solely to avoid filing the claims in the multiple dependent form so as to avoid the additional filing fee.

The claims were not amended in order to address issues of patentability and Applicant respectfully reserves all rights he may have under the Doctrine of Equivalents. Applicant furthermore reserves his right to reintroduce subject matter deleted herein at a later time during the prosecution of this application or continuing applications.

Respectfully submitted,

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APPENDIX

3. (Amended) A method as claimed in claim 1 ~~or 2~~, wherein the data bits selected within one cycle of operation are counted.

5. (Amended) A method as claimed in claim 2 ~~one of the claims 2 to 4~~, wherein the data bits that are already present in the buffer memory which is constructed as a shift register are shifted through the number of new data bits prior to the writing of new data bits.

6. (Amended) A method as claimed in claim 1 ~~one of the preceding claims~~, wherein the selected data bits, possibly already present in the buffer memory, are prepared so as to form an output data word, while utilizing a working bit register which contains m working bits and defines the output format, for output to a memory or the like.

8. (Amended) A method as claimed in claim 6 ~~or 7~~, wherein a predetermined number of data bits is output from the buffer memory.

9. (Amended) A method as claimed in claim 6 ~~one of the claims 6 to 8~~, wherein the data word read out from the buffer memory is extended by the addition of one or more further data bits.

10. (Amended) A method as claimed in claim 6 ~~one of the claims 6 to 9~~, wherein the data word read out from the buffer memory is shifted within the output data word.

11. (Amended) A device for carrying out the method claimed in claim 1 ~~one of the claims 1 to 10~~, including a working processor (2) and a data bit selection unit (1) for selecting

one or more given data bits from a data word (4), comprising n data bits (10), on the basis of a selection bit register (6) which contains n selection bits (11) which indicate whether a data bit (10) of the data word (6) is to be selected, such selection taking place within one cycle of operation of the working processor (2).

13. (Amended) A device as claimed in claim 11 ~~or 12~~, characterized in that there is provided a buffer memory (7) which is constructed as a shift register and in which the data bits (10) selected within one cycle of operation can be stored.

14. (Amended) A device as claimed in claim 11 ~~one of the claims 11 to 13~~, characterized in that there is provided a counter for counting the data bits (10) selected within one cycle of operation and for summing the numbers of bits of a plurality of cycle of operation.

15. (Amended) A device as claimed in claim 13 ~~claims 13 and 14~~, characterized in that data bits already present in the buffer memory (7) can be shifted in dependence on the number of new data bits (10) to be written.

16. (Amended) A device as claimed in claim 11 ~~one of the claims 11 to 15~~, characterized in that there is provided at least one working bit register (8) which contains m working bits (14) and defines the output format, said working bit register preparing data bits read out from the buffer memory (7) so as to be output in the form of an output data word (9).

18. (Amended) A device as claimed in claim 16 ~~or 17~~, characterized in that there is provided a second counter

section (II) which defines the number of data bits (13) to be read out from the buffer memory (7).

19. (Amended) A device as claimed in claim 16 ~~one of the claims 16 to 18~~, characterized in that there is provided a third register section (III) whereby the data bits (15) read out can be shifted within the output data word (9).

20. (Amended) A device as claimed in claim 16 ~~one of the claims 16 to 19~~, characterized in that there are provided a fourth and a fifth register section (IV, V) which define how the output data word (9), consisting of m data bits (15), is to be completed when n data bits are read out from the buffer memory (7), where $n < m$.

21. (Amended) A device as claimed in claim 16 ~~one of the claims 16 to 20~~, characterized in that there is provided a sixth register section (VI) whereby the output mode can be adjusted.

23. (Amended) A device as claimed in claim 11 ~~one of the claims 11 to 22~~, characterized in that it forms part of a portable telecommunication device for mobile telecommunication.